CLAIMS:

1. An electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect through the substrate extending from the first to the second side, on which first side the capacitor is present, characterized in that the capacitor is a vertical trench capacitor provided with a plurality of trenches in which a layer of dielectric material is present between a first and a second conductive surface, said layer of dielectric material also being used as insulation between the substrate and the vertical interconnect.

2. An electronic device as claimed in Claim 1, wherein the vertical interconnect has a first part and a second part, which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape.

3. An electronic device as claimed in Claim 1, characterized in that the trenches of the vertical interconnect are substantially filled with electrically conductive material.

4. An electronic device as claimed in Claim 2, characterized in that the vertical interconnect comprises a plurality of parallel through-holes through the substrate, each of which is filled with electrically conductive material.

5. An electronic device as claimed in Claim 1, characterized in that:
- contact pads for coupling to an external carrier are present on the second side;
- a first vertical interconnect is used for grounding and
- a second interconnect is used for signal transmission.

6. An electronic device as claimed in Claim 4, characterized in that the first and second vertical interconnect are designed so as to form a coaxial structure.

7. An electronic device as claimed in Claim 1, characterized in that an integrated circuit is defined on the second side of the substrate.

8. An electronic device as claimed in Claim 1, characterized in that the substrate comprises a high-ohmic zone which is present adjacent to the vertical capacitors and acts as a protection against parasitic currents.

9. An electronic device as claimed in Claim 1, characterized in that a planar capacitor is present on the first side of the substrate, which planar capacitor comprises the same layer of dielectric material as the vertical capacitor.

10. An assembly comprising the electronic device of any of the preceding Claims, and a semiconductor device, which semiconductor device is electrically connected to bond pads present on the first side of the substrate.

11. A method of manufacturing an electronic device comprising a semiconductor substrate having a first and a second side and provided with a capacitor and a vertical interconnect extending from the first to the second side, on which first side the capacitor is present, said method comprising the steps of:

- providing first trenches in the substrate including the step of etching from the first side of the substrate;
- providing second trenches in the substrate by etching from one side of the substrate and opening the second trenches by removing material from the opposite side of the substrate;
- providing said first trenches with a conductive surface;
- applying a layer of dielectric material on the substrate, covering at least the first side of the substrate and the inner faces of the first and second trenches; and
- applying electrically conductive material in the first trenches and in the second trenches, which conductive material of the first trenches together with the layer of dielectric material and the conductive surface forms the capacitor, and which conductive material of the second trenches forms the vertical interconnects.

12. A method as claimed in Claim 11, wherein the first trenches and the second trenches are etched in a single step, said first trenches having a smaller diameter than the second trenches leading to the through-holes, with the result that the second trenches will extend further into the substrate than the first trenches, said trenches having inner faces.

13. A method as claimed in Claim 12, characterized in that the step of applying conductive material in the second trenches comprises the steps of applying a seed layer and electroplating.

14. A method as claimed in Claim 12, characterized in that a plurality of second trenches are neighbouring and mutually interconnected so as to form a single vertical interconnect.

15. A method as claimed in Claim 14, wherein the electrically conductive material applied in the first and the second trenches is polysilicon.

16. A method as claimed in Claim 11, wherein the step of removing material for opening the second trenches comprises the step of wet-chemical etching to form a cavity, said cavity having a larger diameter than the second trenches.

17. A method as claimed in Claim 11, wherein the second trenches are formed by wet-chemical etching from the second side of the substrate before provision of the first trenches, said second trenches being shaped as cavities and have a larger diameter than the first trenches.

18. A method as claimed in Claim 17, wherein the second trenches are opened by etching in the same step as the etching of the first trenches.

19. A method as claimed in Claim 17, wherein the second trenches extend up to the first side of the semiconductor substrate and are covered by an etch-stop layer provided on the first side of the substrate.